METHOD AND APPARATUS FOR MEMORY MANAGEMENT IN A MULTI-PROCESSOR COMPUTER SYSTEM

ABSTRACT OF THE DISCLOSURE

Improved techniques and systems for accommodating TLB shootdown events in multi-processor computer systems are disclosed. A memory management unit (MMU) having a TLB miss handler and miss exception handler is provided. The MMU receives instructions relative to a virtual address. A TLB is searched for the virtual address, if the virtual address is not found in the TLB, secondary memory assets are searched for a TTE that corresponds to the virtual address and its associated context identifier. The context identifier is tested to determine if the TTE is available. Where the TTE is available, the TLB and secondary memory assets are updated as necessary and the method initiates memory access instructions. Where the TTE is unavailable, the method either resolves the unavailability or waits until the unavailability is resolved and then initiates memory access instructions, thereby enabling the desired virtual address information to be accessed.